DIGITAL 12-BIT C-MOS TELEMETERING SYSTEM FOR SEISMOLOGICAL USE

by

SEPPO NURMINEN

Institute of Seismology, University of Helsinki

Abstract

An economical and reliable digital telemetering system has been developed for data gathering from the seismological network. In this preliminary report, a brief description of the system is given. The subject system is part of a larger project for data centering and modernizing in Finland.

The rate of data transmission is 1200 bits/s in this synchronous binary system.

Introduction

Data can be transmitted over telephone lines in different ways. Either a digital or a frequency modulated system is feasible. The FM system is a very economical and commonly used method, but has drawbacks, e.g. a small dynamic range (about 50—60 dB) and distortion due to variation in phase delay with carrier frequency. This phase delay is several milliseconds, which may be very serious if a small station net is used. The phase delay between the lowest and the highest frequency which can be transmitted on a regular phone line amounts to about 8 milliseconds [3].

Digital telemetering was chosen, because the data have, in any case, to be in digital form at the main station for computer analysis, and digital integrated circuits very suitable for this purpose were available. These digital C-MOS integrated circuits, developed by BCA [1, 2] in the years 1971—73, have a very low input power and a large operating temperature range. With these circuits the design of a low-cost and high-quality digital telemetering system for seismological use was possible.

Data transmission

A 16-bit word is sent over the telephone lines in FM form. Three bits of the word are used for synchronization and one bit for parity checking of the remaining 12 bits. It is possible to choose different sampling rates depending on the number of channels and the transmission rate. For test transmissions we are using one channel taking 75 samples/s at a rate of 1200 bits/s.

Description of the system

The analog voltage from a transducer is amplified by a low-noise low-pass amplifier and sampled and held by a network consisting of a transconductance operational amplifier and a MOS-FET transistor (Fig. 1). This circuit can sample in less than one microsecond and maintain the voltage level over a 10 ms period with a tilt of only a few microvolts. The voltage sampled is converted to digital form by an analog-to-digital converter (Fig. 3).

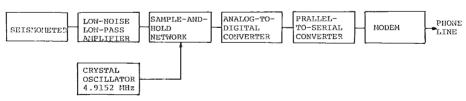


Fig. 1. Telemetering transmitter.

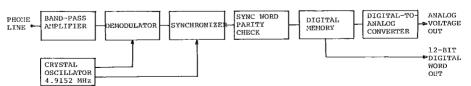


Figure 2. Telemetering receiver.

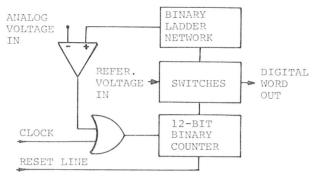


Fig. 3. The counter ramp analog-to-digital converter.

There are many methods for digitizing an analog signal [4]. We chose the counter ramp method. This A/D converter constructed of C-MOS circuits takes about 1 ms to convert a 12-bit word. That time is convenient in this telemetering system, as the sampling interval never needs to be below 2 ms, and the sample-and-hold network keeps the analog level unchanged during the digitizing process; accordingly, the uncertainty error is nil. Moreover, this type of A/D converter gives high accuracy and reliability at low cost.

The digital parallel word from the A/D converter is converted to serial form and combined with a parity bit and a three-bit synchronizing word. This serial form data is frequency-modulated and, after filtering, is fed to the telephone line.

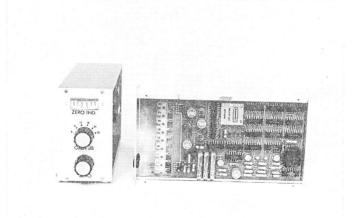


Fig. 4. The digital telemetering receiver and transmitter.

The FM information from the telephone line is amplified and led through a band-pass filter (Fig. 2). A special digital demodulator measures every pulse which passes the band-pass filter, draws conclusions from the time differences between pulses, and converts the output of the demodulator to a state corresponding to the time differences of the mark or space in FM transmission. A crystal oscillator is synchronized by this demodulated data, so that every data shift changes the clock phase 1/64 part, if necessary.

The serial form data with the clock signal is fed to a parallel converter. At first this 16-bit word is analyzed all the time until the synchronizing word and the right parity bit are found. This synchronized word is triggered to a memory circuit, from which the digital 12-bit word is converted to analog form.

Next time the sync and parity check takes place after a 16-bit interval. If no sync word is found, everything starts again from the beginning; but if only the parity bit is wrong, then that word is not read to the memory, but the word synchronization will remain.

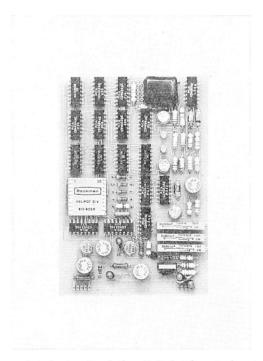


Fig. 5. The printed circuit of the digital telemetering transmitter.

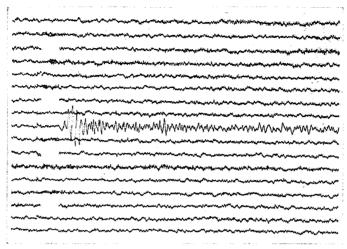


Fig. 6. An analog record of the digital test transmission.

Discussion

The telemetering system has been tested during several months. The overall accuracy is 1/2 LSB (half of the least significant bit) and the system works satisfactorily at temperatures from -20 to $+40^{\circ}$ C. We have not yet had an opportunity to test the system below -20° C or over $+40^{\circ}$ C, but, according to the data sheet specifications of these circuits, it should still work.

The input current of the transmitter, including the seismic amplifier, the A/D converter and the modem, is 6 mA from a 12 V battery. In our tests we have managed to keep the transmitter operating satisfactorily even at 10 mW input power. Thus a small battery lasts several months in this transmitter.

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